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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,294	04/21/2005	Hermana Wilhelmina Hendrika De Groot	NL02 1047 US	8636

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EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauman et al, US. Pat. No. 5,915,128.

3. Claims 1, 6-10, Bauman teaches a device for exchanging data signals between a first clock domain and a second clock domain [*serial speed matching buffer*], characterized in that the device comprises a serial memory element [*when the registers in the chain are put into a serial shift mode, see col. 3, lines 32-35*] and a parallel memory element coupled to the serial memory element the serial memory element [*col. 16, lines 51-55*] comprising at least one memory location more for the data signals than the parallel memory element [*see Figs. 6A and 6B and related discussion*].

4. Claim 2, Bauman teaches the serial memory element is arranged for writing the data signals and the parallel memory element is arranged for reading out the data signals [*col. 3, lines 22-38*].

5. Claim 3, Bauman teaches a first control signal for writing the data signals in the serial memory element can be derived from a first clock signal which is arranged for synchronizing the data signals in the first clock domain, and in that a second control signal for reading the data signals from the parallel memory element can be derived from a second clock signal which is

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arranged for synchronizing the data signals in the second clock domain [*phase 1 Clock and phase 2 Clock of Fig. 2*].

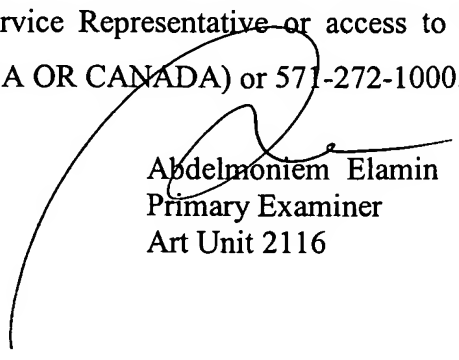
6. Claims 4-5, Bauman teaches the serial memory element is arranged for reading out the data signals and in that the parallel memory element is arranged for writing the data signals [*col. 3, lines 22-38*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdelmoniem Elamin whose telephone number is 571-2727-3674. The examiner can normally be reached on MON - THUR 10:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Abdelmoniem Elamin
Primary Examiner
Art Unit 2116

August 20, 2006